



PUMB24

50 V, 20 mA PNP/PNP resistor-equipped transistor;
R1 = 100 k Ω , R2 = 100 k Ω

10 July 2023

Product data sheet

1. General description

PNP/PNP Resistor-Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD)plastic package.

NPN/NPN complement: PUMH24

NPN/PNP complement: PUMD24

2. Features and benefits

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place cost
- AEC-Q101 qualified

3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replacement of general-purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

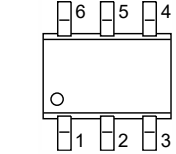
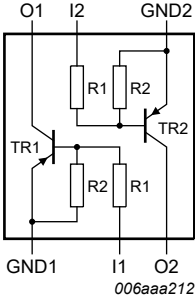
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor							
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V	
I _O	output current		-	-	-20	mA	
R1	bias resistor 1 (input)		[1]	70	100	130	k Ω
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	

[1] See Section "Test information" for resistor calculation and test conditions.

50 V, 20 mA PNP/PNP resistor-equipped transistor; R1 = 100 k Ω , R2 = 100 k Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>TSSOP6 (SOT363)</p>	 <p>006aaa212</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMB24	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PUMB24	T7%

[1] % = placeholder for manufacturing site code

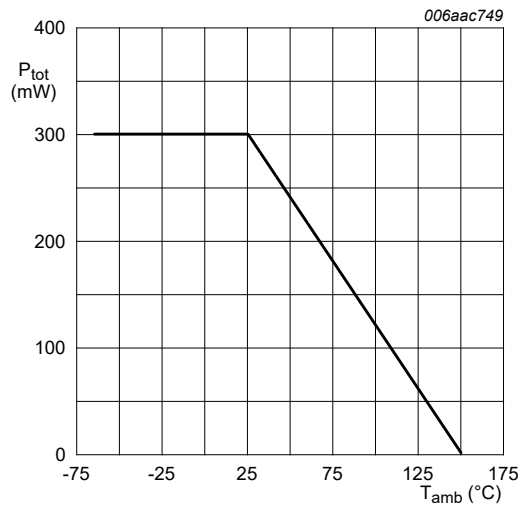
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{CBO}	collector-base voltage	open emitter		-	-50	V
V_{CEO}	collector-emitter voltage	open base		-	-50	V
V_{EBO}	emitter-base voltage	open collector		-	-10	V
V_I	input voltage			-40	10	V
I_O	output current			-	-20	mA
I_{CM}	peak collector current			-	-100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

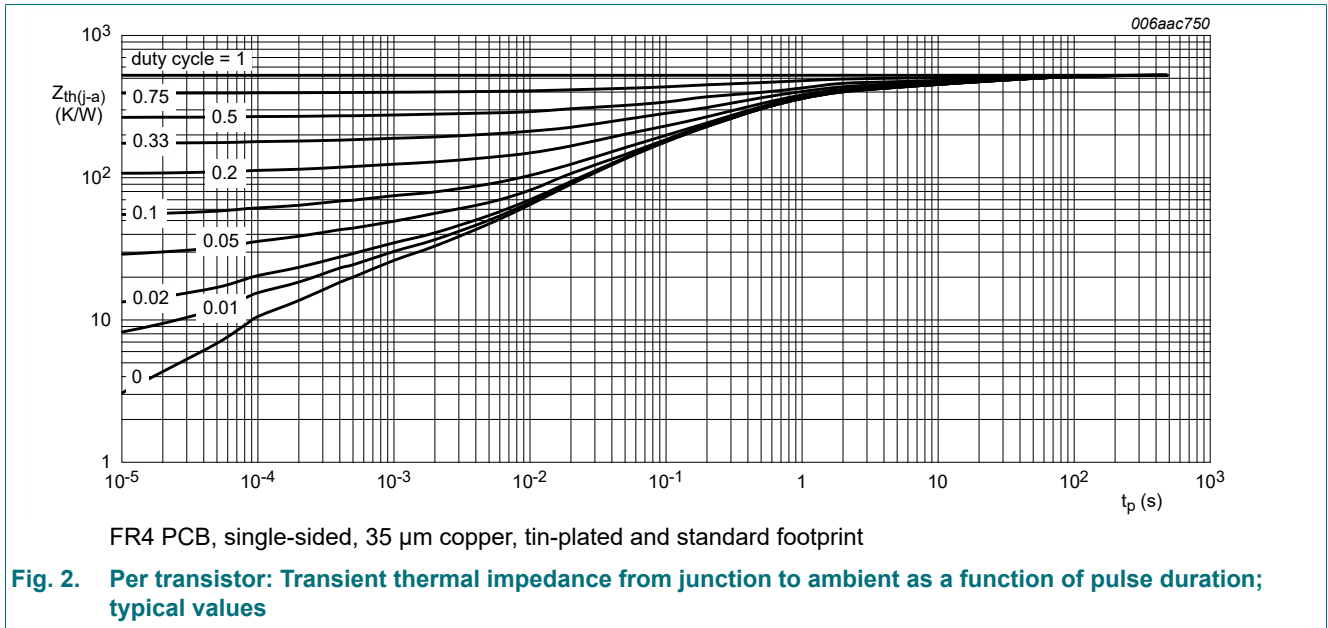
Fig. 1. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	416	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.

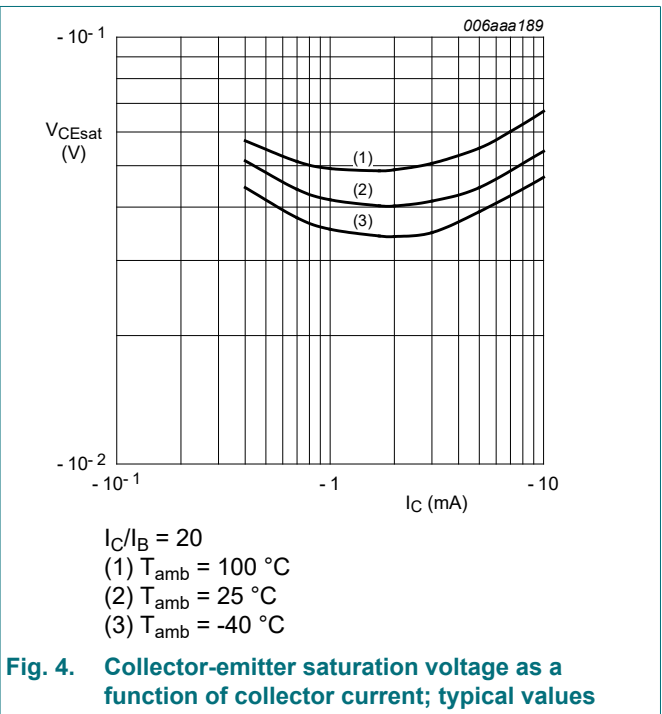
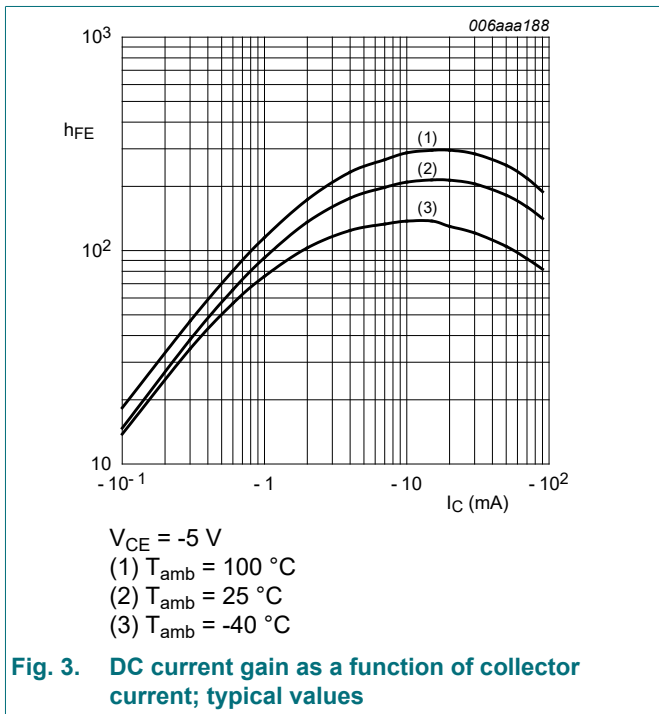


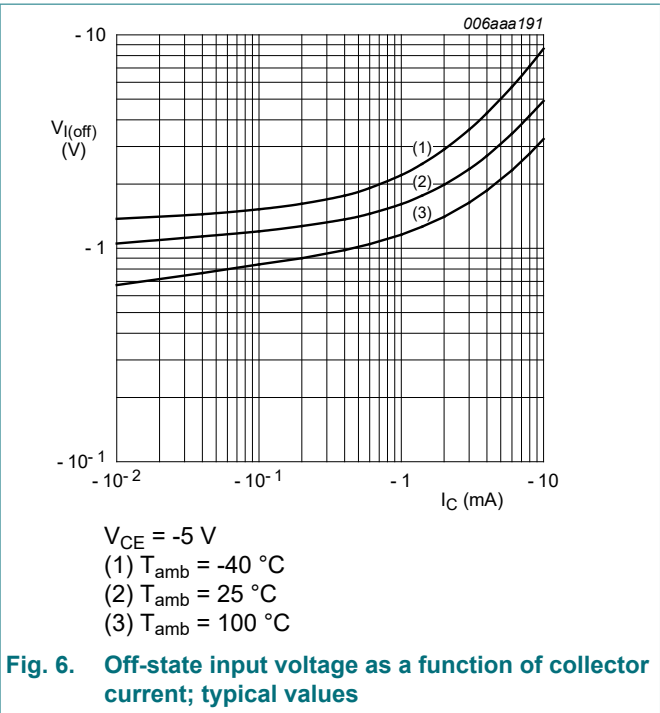
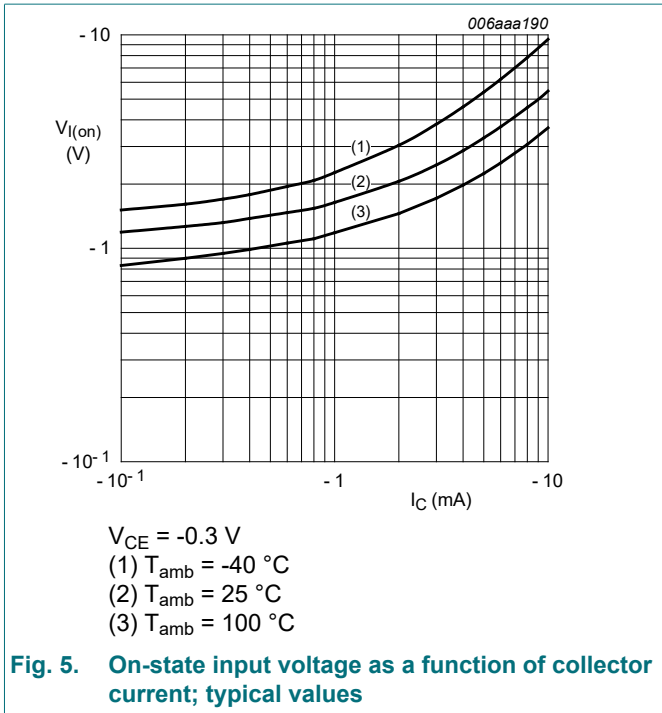
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = -100 \mu A$; $I_E = 0 A$; $T_{amb} = 25 \text{ }^\circ C$	-50	-	-	V	
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = -2 \text{ mA}$; $I_B = 0 A$; $T_{amb} = 25 \text{ }^\circ C$	-50	-	-	V	
I_{CBO}	collector-base cut-off current	$V_{CB} = -50 \text{ V}$; $I_E = 0 A$; $T_{amb} = 25 \text{ }^\circ C$	-	-	-100	nA	
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30 \text{ V}$; $I_B = 0 A$; $T_{amb} = 25 \text{ }^\circ C$	-	-	-100	nA	
		$V_{CE} = -30 \text{ V}$; $I_B = 0 A$; $T_j = 150 \text{ }^\circ C$	-	-	-5	μA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}$; $I_C = 0 A$; $T_{amb} = 25 \text{ }^\circ C$	-	-	-50	μA	
h_{FE}	DC current gain	$V_{CE} = -5 \text{ V}$; $I_C = -5 \text{ mA}$; $T_{amb} = 25 \text{ }^\circ C$	80	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = -5 \text{ mA}$; $I_B = -0.25 \text{ mA}$; $T_{amb} = 25 \text{ }^\circ C$	-	-	-150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5 \text{ V}$; $I_C = -100 \mu A$; $T_{amb} = 25 \text{ }^\circ C$	-	-1.2	-0.5	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3 \text{ V}$; $I_C = -1 \text{ mA}$; $T_{amb} = 25 \text{ }^\circ C$	-3	-1.6	-	V	
R1	bias resistor 1 (input)		[1]	70	100	130	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = -10 \text{ V}$; $I_E = 0 A$; $i_e = 0 A$; $f = 1 \text{ MHz}$; $T_{amb} = 25 \text{ }^\circ C$	-	-	2.5	pF	

[1] See Section "Test information" for resistor calculation and test conditions.





11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

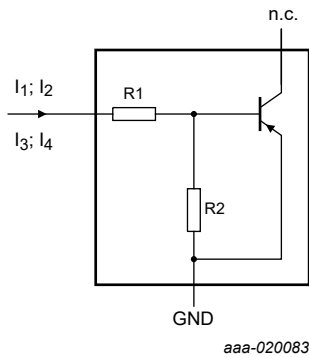


Fig. 7. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
PUMB24	100	100	-20 μA	-60 μA	20 μA	40 μA

12. Package outline

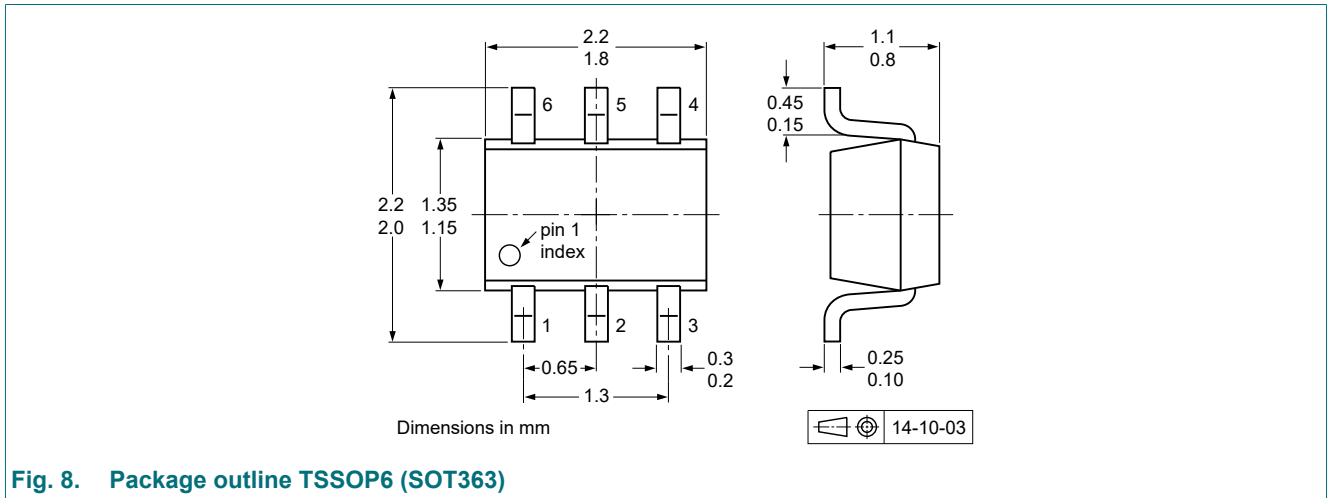


Fig. 8. Package outline TSSOP6 (SOT363)

13. Soldering

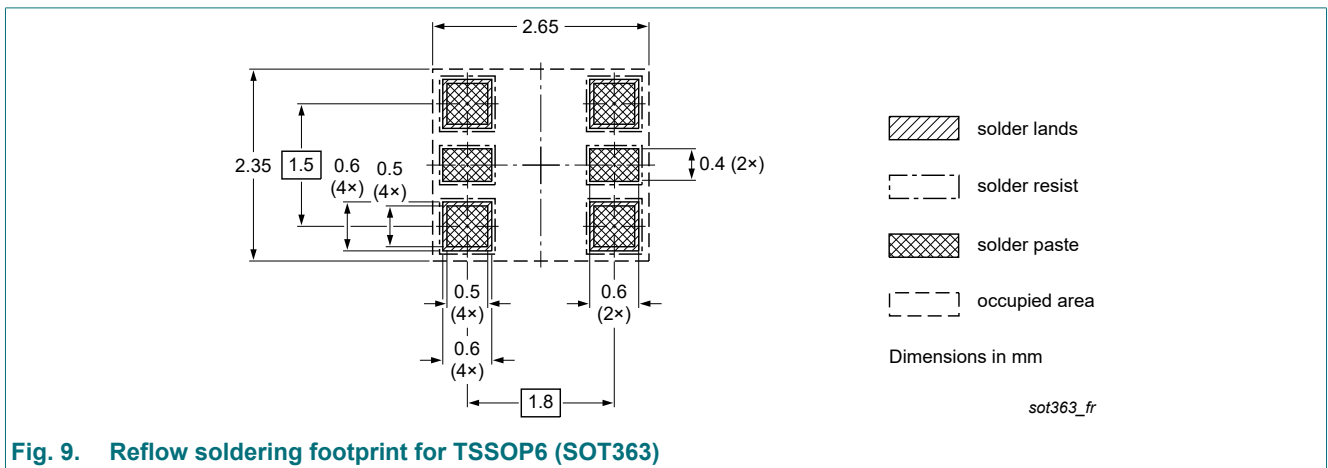


Fig. 9. Reflow soldering footprint for TSSOP6 (SOT363)

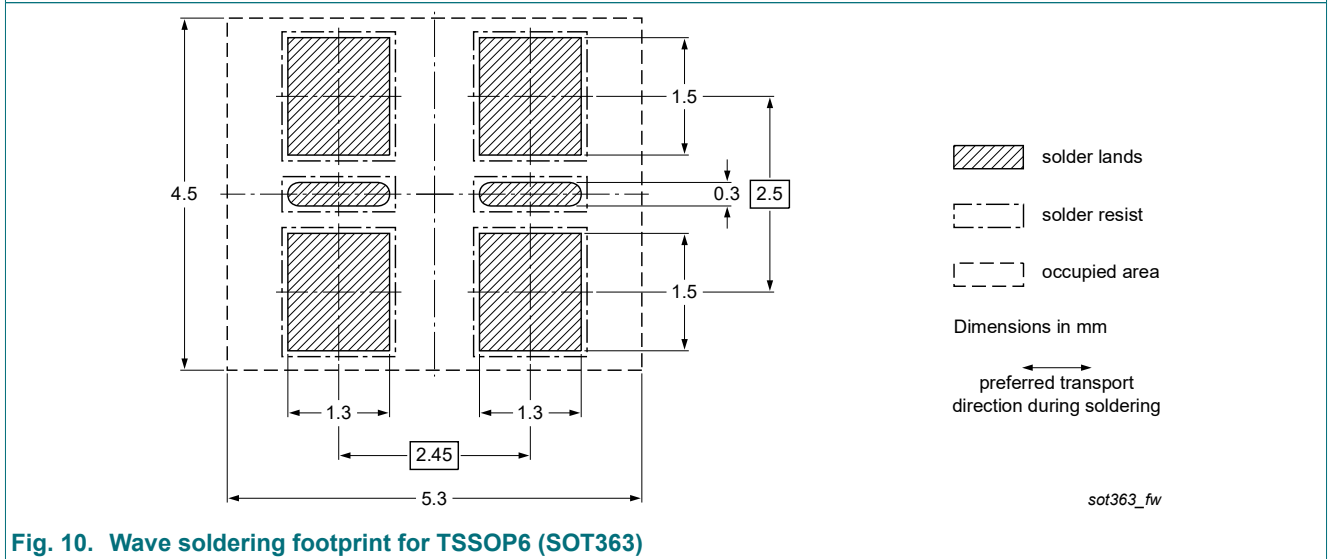


Fig. 10. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMB24 v.3	20230710	Product data sheet	-	PEMB24_PUMB24_2
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.• Legal texts have been adapted to the new company name where appropriate.• Family data sheet reduced to single type data sheet.• Package information removed.			
PEMB24_PUMB24_2	20090902	Product data sheet	-	PEMB24_PUMB24_1
PEMB24_PUMB24_1	20050218	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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